REMARKS/ARGUMENTS

Claims 1-18 are pending in the subject application and each has been rejected in the subject Office action. No claim amendments are filed herein.

Applicants respectfully request reconsideration and allowance of each of pending claims 1-18.

I. Rejection of Claims 1, 3-5, 9, 14-15, 17 and 18 under 35 U.S.C. § 103

In paragraph 2 of the subject Office action, claims 1, 3-5, 9 and 14-15, 17 and 18 were rejected under 35 U.S.C § 103(a) as being unpatentable over Clark et al. (U.S. Pat. No. 6,767,793), hereinafter "Clark" in view of Fried et al, (USPUB 2003/0113970), hereinafter "Fried." Applicants respectfully submit that these claim rejections are overcome for reasons set forth below.

Each of independent claims 1 and 17 provides a gate electrode over the top of a semiconductor fin device. In particular, each claim recites a fin device with a coating of a thin film of gate dielectric on the top and the opposed sides of the fin. Each claim also recites a gate electrode material formed over the fin. The gate electrode material has a planar upper surface and extends past the opposed sides of the fin device and above the top of the fin device. Because the gate electrode material is formed over and extending past the opposed sides of the fin device coated with a gate dielectric on its top and opposed sides, each of claims 1 and 17 also provide:

> "the top and the opposed sides of the semiconductor device each form a channel portion of a single associated transistor."

The claimed invention of claims 1 and 17 is therefore distinguished from the **Clark** reference because, in the Clark reference, gate electrode material does not extend over the top of the alleged fin.

The claimed invention of claims 1 and 17 is also distinguished from the **Fried** reference because, in the Fried reference, two distinct transistors are formed on

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opposed sides of the alleged fin and there is no channel formed on the top surface of the fin.

In summary, neither of the references nor the combination thereof, provides the claimed features of a fin with a gate dielectric that extends along the sides and over the top of the fin and a gate electrode material with a planar top surface that is formed over and on opposed sides of, the fin providing a single transistor channel extending along the opposed sides and along the top of the fin.

*** Clark reference**

In FIG. 31, Clark provides an SiGe layer 300 with thermal oxide 320 formed there-over and along its sides. Gate conductor 310 is disposed only lateral to SiGe layer 300 and clearly does not extend over SiGe layer 300 nor the portion of thermal oxide 320 that is on top of the SiGe layer 300. In the *Response to Arguments* section of the subject Office action, Applicants believe that the Examiner misstates the argument presented by Applicants in Applicants' previously-filed Response of August 9, 2007, by stating that "Applicant argues that Clark does not disclose a gate electrode disposed opposite the thermal oxide 320," page 8, lines 7-8. Actually, Applicants argued that "*The top portion of structure* 300 of Clark therefore does not form a channel because there is no gate electrode disposed opposite the thermal oxide layer 320." (In order for a channel to exist along the top of the fin, a gate electrode must be disposed opposite the gate dielectric at that location.) Moreover, this feature that a channel is formed on top of the fin is reflected in the language of claims 1 and 17 and distinguishes Applicants' invention from Clark which is lacking a gate electrode material over structure 300.

Further, on page 8 of the subject Office action, lines 8-10, the Examiner continues "However 310, fig. 31 is gate electrodes disposed opposite the thermal oxide 320, see col. 7, lns. 50-57. *Therefore, Clark reads on the amended claim*" (emphasis added). However, the Examiner had conceded on page 4 of the subject Office action

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that "Clark does not disclose the limitation(s) of claims 1 and 17." Portions of claims 1 and 17 then follow without the specific alleged deficiency of Clark being identified but the Office action continues with "However, Fried discloses: Claims 1 and 17: planarizing the layer of gate electrode material (32, fig. 5B), to produce a substantially planar surface formed only of the gate electrode material disposed atop the semiconductor device and extending past each of the opposed sides . . ." in the paragraph bridging pages 4 and 5.

Applicants are therefore unsure of the Examiner's position, but respectfully submit that it is clear that Clark does not provide a gate electrode over the top of the fin, much less over the top of a gate dielectric formed over the fin, much less a channel of a transistor formed in the top of the fin (with other portions of the channel of the same transistor being along the sides of the fin).

Claim 17 and claim 1 are clearly distinguished from Clark.

*** <u>Fried reference</u>**

Fried does not disclose the claimed feature of "gate electrode material disposed atop the semiconductor device" (claim 1) or "gate electrode material . . . disposed atop the gate dielectric film formed over the top of the fin" (claim 17) and Fried clearly does not disclose the feature of "the top and the opposed sides of the semiconductor device each form a channel portion of a single associated transistor" (claims 1,17).

Fried is clearly directed to providing an asymmetrical FINFET - two separate transistors of opposite polarity formed on the opposed sides of the fin structure 12 as in FIG. 5B. A P-gate transistor is formed on one side of the fin with an N-gate transistor formed on the opposite side. Gate dielectric 16 does not extend over the top of fin 12. The gate material 24, 26 does not extend over fin 12 and a transistor channel is not formed over the top of fin 12 because hardmask 14 is disposed over fin 12, precluding a transistor channel from being formed on top of fin 12. There is no suggestion in Fried to utilize the top portion of the fin as a channel or portion of the channel because the

transistors formed on opposed sides of the fin are distinct and of opposite polarity. Indeed, the Fried disclosure is directed to the features of an asymmetrical device with opposed n-type and p-type gates and the hardmask formed on top of the fin, together with the absence of gate electrode material atop the fin, helps separate the two distinct transistors. Fried *teaches away* from a single transistor having a channel that extends along opposed sides and over top of a fin device.

Independent claims 1 and 17 are therefore distinguished from the references of Clark and Fried, taken alone or in combination. The rejection of claims 1, 3-5, 9, 14-15, 17 and 18 in this section should be withdrawn because claims 3-5, 9 and 14-15 depend from claim 1 and also because claim 18 depends from claim 17.

II. Rejection of Claims 2, 6-8 and 17

In paragraph 4 of the subject Office action, claims 2, 6-8 and 17 were rejected under 35 U.S.C § 103(a) as being unpatentable over Clark in view of Fried as applied to claims 1 and 17, and further in view of Kinsbron (U.S. Pat. No. 4,432,132). Applicants respectfully submit that these claim rejections are overcome for reasons set forth below.

As previously stated, Kinsbron merely stands for the proposition that a photoresist layer has a planar top surface and will be of uniform thickness when applied over a planar surface. Kinsbron does not make up for the above-stated deficiencies of Clark in view of Fried and therefore independent claims 1 and 17 as well as dependent claims 2, and 6-8, are distinguished from the references of Clark, Fried and Kinsbron, taken alone or in combination.

The rejection of claims 2, 6-8 and 17 under 35 U.S.C § 103(a), should therefore be withdrawn.

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III. Rejection of Claims 10-13

In paragraph 5 of the subject Office action, claims 10-13 were rejected under 35 U.S.C § 103(a) as being unpatentable over Clark in view of Fried as applied to claim 1, and further in view of Fried et al. (USP 6,657,252), hereinafter "Fried II". Applicants respectfully submit that these claim rejections are overcome for reasons set forth below.

As above, claim 1 is distinguished from Clark and Fried and claims 10-13, which depend from claim 1, are similarly distinguished. Fried II has apparently been relied upon for providing a gate dielectric material including silicon oxynitride, a high permittivity material and a thickness in the range of 3-100 angstroms. Fried II does not make up for the above-stated deficiencies of the combination of Clark and Fried. Because Fried II does not make up for these deficiencies, claim 1 and therefore dependent claims 10-13 are distinguished from the references of Clark, Fried and Fried II, taken alone or in combination.

The rejection of claims 10-13 under 35 U.S.C. § 103(a) as being unpatentable over Clark in view of Fried and further in view of Fried II, should therefore be withdrawn.

IV. Rejection of Claim 16

In paragraph 6 of the subject Office action, claim 16 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Clark in view of Fried and further in view of Achuthan, et al. (U.S. 6,855,607). Applicants respectfully submit that this claim rejection is overcome for reasons set forth below.

Claim 16 depends from claim 1, which is distinguished from Clark and Fried, as above. Achuthan, et al. has apparently been relied upon for providing the multiple gate electrode being formed of a metal material. Achuthan et al., however, does not make up for the above-stated deficiencies of Clark and Fried. In particular, Achuthan does not provide a gate electrode material with a planar top surface atop the semiconductor device and extending distally past each of the opposed sides. Because Achuthan does not make up for the above-stated deficiencies of Clark and Fried, independent claim 1

and therefore dependent claim 16 are both distinguished from Clark and Fried in view of Achuthan, et al. As such, the rejection of claim 16 under 35 U.S.C. § 103(a), should be withdrawn.

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CONCLUSION

Based on the foregoing, Applicants respectfully submit that each of claims 1-18 is in allowable form and the application is therefore in condition for allowance, which action is expeditiously and respectfully requested by Applicants.

The Assistant Commissioner for Patents is hereby authorized to charge any fees or credit any excess payment that may associated with this communication, to Deposit Account 04-1679.

Respectfully submitted,

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